

## Module Specification

### Module Summary Information

<b>1</b>	<b>Module Title</b>	Analogue Microelectronics and Integrated Circuit Architecture
<b>2</b>	<b>Module Credits</b>	20
<b>3</b>	<b>Module Level</b>	7
<b>4</b>	<b>Module Code</b>	ENG7157

<b>5</b>	<b>Module Overview</b>
<p><b>Rationale</b></p> <p>This module introduces the key integrated circuit techniques for BJT and MOS design, starting with transistor circuits (current mirrors, long tail pairs, amplifier stages, buffers) and extend your knowledge and expertise into analyse and design basic analogue microelectronic building blocks at the circuit level, with an emphasis towards integrated circuit architecture with applications in communications circuits. The circuits will be developed using schematic and simulation design techniques to enable analogue circuits and systems to be implemented. The circuit elements will then be extended to cover current sources, CMOS and BiCMOS circuits and current mode circuits. These building blocks will then be expanded into useful system level blocks such as phase locked loops, integrated circuit architecture and communications IC architecture. Fundamentally important issues such as noise, IC architecture and power consumption will also be covered in this module.</p>	

<b>6</b>	<b>Indicative Content</b>
<p>Review of BJT and MOST device used in circuit simulation. BJT and MOST noise Models.</p> <p>BJT and MOST amplifier circuits, use of active model parameters, pole-zero, frequency response and noise.</p> <p>Negative feedback amplifier circuits, type of feedback connection, loading efforts, analysis of amplifier closed loop characteristics.</p> <p>Signal processing circuits op-amps, closed-loop frequency stability from a systems prospective.</p> <p>Basic integrated circuit building blocks, current sources and current mirror circuits.        Large and small-signal design of MOS/CMOS and BiCMOS OTA's, the folded cascode OTA, the output buffer; pole-zero, bandwidth, GBW, stability, load and Miller compensation techniques, slew-rate, systematic offset, random offset, PSRR and noise considerations. The comparator, delay, Weak threshold region of operation, low power OTA'S.</p> <p>Introduction to current-mode circuits for analogue design.</p> <p>IC architectural design and applications and switch capacitor circuit threshold.</p>	

**Communications IC Architecture I – IC level design of wireless communications building blocks including translinear: Gilbert cell, multiplier circuits, transconductance.**

- Communications IC Architecture I – IC level design of wireless communications building blocks including translinear: Gilbert cell, multiplier circuits, transconductance.
- Communications IC Architecture II – IC level design of optical communications building blocks, including transmitter and receiver, clock and data recovery.
- Tutorial 12 – PC-ECAD tutorial session

<b>7</b>		<b>Module Learning Outcomes</b>
<b>On successful completion of the module, students will be able to:</b>		
	<b>1</b>	Critically evaluate the technology of existing analogue systems and be able to specify the most appropriate solutions for a variety of requirements.
	<b>2</b>	Critically analyse and design analogue circuit building blocks and review their performance.
	<b>3</b>	Critically assess the performance of analogue feedback systems for noise, stability and bandwidth.
	<b>4</b>	Describe current-mode integrate circuit architectures for various analogue signal processing functions.

<b>8</b>		<b>Module Assessment</b>		
<b>Learning Outcome</b>				
		<b>Coursework</b>	<b>Exam</b>	<b>In-Person</b>
<b>1-4</b>			<b>X</b>	

<b>9</b>		<b>Breakdown Learning and Teaching Activities</b>
<b>Learning Activities</b>	<b>Hours</b>	
<b>Scheduled Learning (SL)</b> includes lectures, practical classes and workshops, peer group learning, Graduate+, as specified in timetable	36	
<b>Directed Learning (DL)</b> includes placements, work-based learning, external visits, on-line activity, Graduate+, peer learning, as directed on VLE	N/A	
<b>Private Study (PS)</b> includes preparation for exams	164	
<b>Total Study Hours:</b>	200	